ANALOG DEVICES

Precision Instrumentation Amplifier

AD624

1.1 Scope.

This specification covers the detail requirements for a programmable gain instrumentation amplifier. The gain equation is $\frac{40{,}000}{R_G} + 1 \pm 20\%$ with external resistor gain programming.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD624SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-16.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	±18V
Internal Power Dissipation	280mW
Rated Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 22°C/W
θ_{JA} = 95°C/W

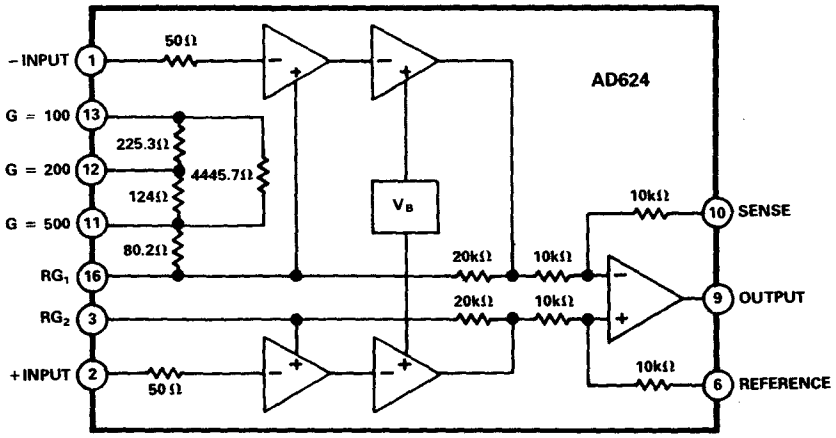
AD624 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Gain Error 1	GE_1	−1	0.05	0.05			G = 1, V_O = ±10V	±% max
Gain Error 100	GE_{100}	−1	0.25	0.25			G = 100, V_O = ±10V	±% max
Gain Error 200	GE_{200}	−1	0.5	0.5			G = 200, V_O = ±10V	±% max
Gain Error 500	GE_{500}	−1	0.5	0.5			G = 500, V_O = ±10V	±% max
Gain Error Drift 1	$TCGE_1$	−1	5				G = 1, V_O = ±10V	±ppm/°C max
Gain Error Drift 100	$TCGE_{100}$	−1	10				G = 100, V_O = ±10V	±ppm/°C max
Gain Error Drift 200	$TCGE_{200}$	−1	10				G = 200, V_O = ±10V	±ppm/°C max
Gain Error Drift 500	$TCGE_{500}$	−1	15				G = 500, V_O = ±10V	±ppm/°C max
Input Offset Voltage	V_{OSI}	−1	75	75			V_{IN} = 0V	±μV max
Input Offset Voltage Drift	TCV_{OSI}	−1	2		2		G = 500, V_{IN} = 0V	±μV/°C max
Output Offset Voltage	V_{OSO}	−1	3	3			V_{IN} = 0V	±mV max
Output Offset Drift	TCV_{OSO}	−1	50		50		G = 1, V_{IN} = 0V	±μV/°C max
Input Bias Current	I_B	−1	50	50			G = 1	±nA max
Input Offset Current	I_{OS}	−1	35	35			G = 1	±nA max
Common-Mode Rejection	$+CMRR_1$	−1	70	70			G = 1, V_{IN} = 0V to +10V	dB min
Common-Mode Rejection	$-CMRR_1$	−1	70	70			G = 1, V_{IN} = 0V to −10V	dB min
Common-Mode Rejection	$+CMRR_{100}$	−1	100	100			G = 100, V_{IN} = 0V to +10V	dB min
Common-Mode Rejection	$-CMRR_{100}$	−1	100	100			G = 100, V_{IN} = 0V to −10V	dB min
Common-Mode Rejection	$+CMRR_{200}$	−1	100	100			G = 200, V_{IN} = 0V to +10V	dB min
Common-Mode Rejection	$-CMRR_{200}$	−1	100	100			G = 200, V_{IN} = 0V to −10V	dB min
Common-Mode Rejection	$+CMRR_{500}$	−1	110	110			G = 500, V_{IN} = 0V to +10V	dB min
Common-Mode Rejection	$-CMRR_{500}$	−1	110	110			G = 500, V_{IN} = 0V to −10V	dB min
Power Supply Current	I_{CC}	−1	5	5			G = 1	mA max
Power Supply Rejection	$PSRR_1$	−1	75	75			G = 1, V_S = ±12V, ±15V	dB min
Power Supply Rejection	$PSRR_{100}$	−1	105	105			G = 100, V_S = ±12V, ±15V	dB min
Power Supply Rejection	$PSRR_{200}$	−1	105	105			G = 200, V_S = ±12V, ±15V	dB min
Power Supply Rejection	$PSRR_{500}$	−1	110	110			G = 500, V_S = ±12V, ±15V	dB min

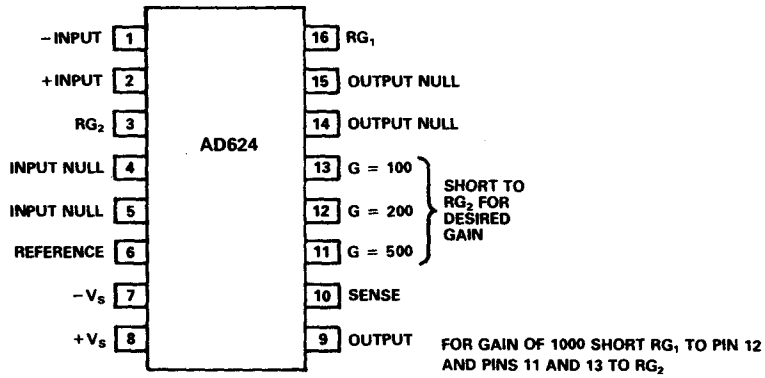
NOTE
[1]V_S = ±15V, R_L = 2kΩ unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).